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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date

Jan. 8, 2008

Beverly Loken

Beverly Loken

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Tim Murphy and Lee Gotcher

Attorney Docket No.: 501039.04

Patent No. : US 7,015,599 B2

Serial No. : 10/652,066

Issue Date : March 21, 2006

Filed : August 29, 2003

Title : METHOD AND SYSTEM FOR ELECTRICALLY COUPLING A CHIP TO CHIP
PACKAGE

REQUEST FOR CERTIFICATE OF CORRECTION

Certificate

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

JAN 14 2008

of Correction

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line

Reads

Should Read

Column 5, Lines 16-
17 and 19

"electromagnetic signals
107,105,104"

--electromagnetic signals **107, 105,**
104--

Column 5, Line 52

"signals **131**, and"

--signals **131** and--

Column 6, Lines 34-
36

"a memory-cell array coupled
to the address decoder,
control circuit, and read/write
circuit, the memory-cell array;
and"

--a memory cell array coupled to
the address decoder, control
circuit, and read/write circuit;
and--

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Column 7, Line 2 "converter mounted on the
chip" --converter is mounted on the
chip--

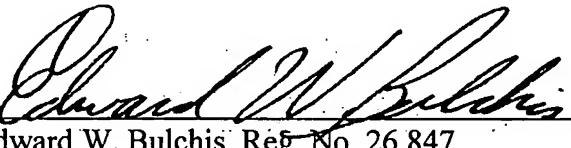
The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: Jan. 7, 2008

By: 

Edward W. Bulchis, Reg. No. 26,847
Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
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Attorney for Applicant(s).

EWB:tdp

Enclosures:

Postcard
Form PTO-1050 (+ copy)

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UNITED STATES PATENT AND TRADEMARK OFFICE
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<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Column 5, Lines 16-17 and 19	"electromagnetic signals 107,105,104"	--electromagnetic signals 107, 105, 104--
Column 5, Line 52	"signals 131, and"	--signals 131 and--
Column 6, Lines 34-36	"a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array; and"	--a memory cell array coupled to the address decoder, control circuit, and read/write circuit; and--
Column 7, Line 2	"converter mounted on the chip"	--converter is mounted on the chip--

MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101

Patent No. US 7,015,599 B2

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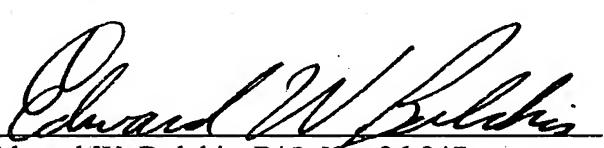
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